Machine Vision **Components** for Image **Acquisition**, **Analysis** and **Transport**

sensor to image

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Who are we?

Sensor to Image is the world leader in industrial camera interface IP supporting GigEVision, USB3-Vision and CoaXPress with more than 150 customers around the world.

Sensor to Image is serving the technical committees of GigEVision & USB3 vision and GenICam for more than 10 years, and coauthoring the CoaXPress standard for 5 years.

Based in Schongau (Germany), Sensor to Image GmbH is a machine vision specialist who develops and sells FPGA-based imaging and video IP Core and products. Its expertise encompasses the GenICam, GigE Vision, CoaXPress, USB3 Vision and MIPI standards, as well as the Xilinx and Intel/Altera platforms.

Starting in 1989, the company has built a reputable know-how in modular PC image processing cards for industrial purposes. Its journey started with the Snofru and Giseh cards, which allowed for PC-independent evaluation of camera signals.

Since 2017, Sensor to Image is part of Euresys and benefits from the group's global reach and extensive distribution and support network.

Today, Sensor to Image main products are GigE Vision, CoaXPress and USB3 Vision IP Cores, as well as IMX Pregius and MIPI IP Cores. They are compatible with Xilinx and Intel/Altera FPGAs. They minimize camera and embedded system development time while offering high performance in a small footprint. Its Vision Standard IP Cores are certified by the AIA and the JIIA and Sensor to Image is an active member of these associations.

Sensor to Image has supplied more than 100 customers around the world in the automotive, industrial, medical, security, military and space application fields.

Sensor to Image is a member of the Xilinx Partner Program since 2007 and an Intel Solution Partner.

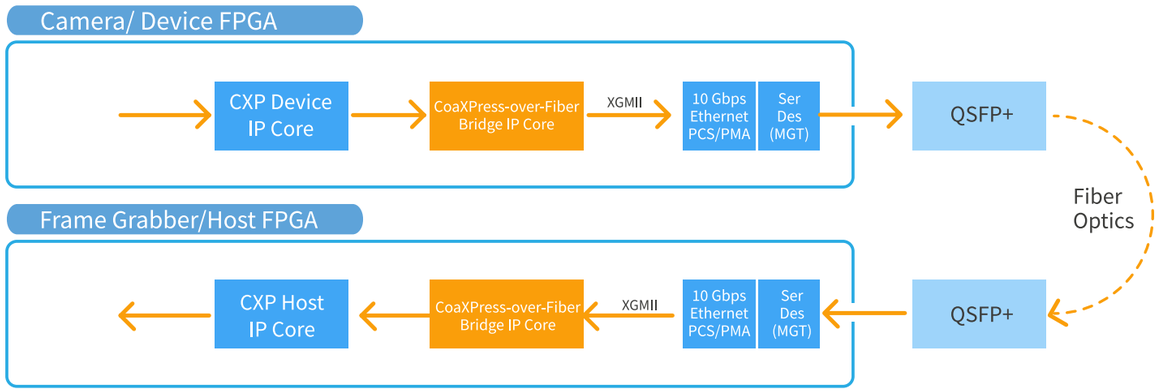
CoaxPress-over-Fiber Bridge IP Core

CXP over-Fiber

COAXPRESS-OVER-FIBER BRIDGE IP CORE FOR FPGA

AT A GLANCE

- Available as CXP to XGMII (device) or XGMII to CXP (host) Bridge IP Cores
- Compatible with Xilinx 7 Series (and newer), Intel Cyclone/Arria 10 and Microchip PolarFire devices
- Compatible with S2I and third-party CoaXPress IP Cores
- Delivered with a working reference design (when licensed with the S2I CoaXPress IP Core)



Description

The CoaXPress-over-Fiber Bridge IP Core allows to connect a CoaXPress IP Core to an XGMII (10 Gbps Media Independent Interface) bus inside an FPGA. XGMII, as defined in IEEE Std 802.3 Clause 46, is the main access to the 10G Ethernet physical layer. The generic nature of this interface facilitates mapping the CoaXPress signaling into the PCS/PMA Ethernet sublayers.

S2I's CoaXPress-over-Fiber Bridge IP Core is available as a device or host version. In a camera (device), it converts CoaXPress packets to XGMII packets going towards an Ethernet PCS/PMA block. In a frame grabber (host), it converts XGMII packets to CoaXPress packets.

What is CoaXPress-over-Fiber?

CoaXPress-over-Fiber is a light but significant extension of the existing CoaXPress specification to support transport over fiber optics.

CoaXPress (CXP) is the de-facto standard for high-bandwidth computer vision applications. CoaXPress 2.1, the latest version of the specification, specifies the CXP 12 speed, a 12.5 Gbps (Gigabit per second) connection over a coaxial copper cable. As link aggregation is common with CoaXPress, bandwidths of 50 Gbps (12.5 x 4) are easily achievable with four CXP-12 connections. The CoaXPress specification is hosted by the JIIA (Japan Industrial Imaging Association).

CoaXPress-over-Fiber has been designed as an add-on to the CoaXPress specification. It provides a way to run the CoaXPress protocol, as it is, unmodified, over a standard Ethernet connection, including fiber optics. As such, CoaXPress-over-Fiber uses standard electronics, connectors and cables designed for Ethernet, but the protocol is CoaXPress, not Ethernet, not GigE Vision.

What are the benefits of using CoaXPress-over-Fiber for my application?

- Ultra-high data/frame rates
- Many accessory and cabling options to cover any length requirement
- Low CPU overhead, low latency, low jitter image acquisition
- Highest camera count per PC performance
- Very competitive cost/performance ratio
- Wide industry acceptance due to JIIA and IEEE standardization

GigE Vision IP Core

GIGE VISION IP CORE FOR FPGA

AT A GLANCE

- Compatible with Xilinx 7 Series (and higher) and Intel Cyclone V devices (and higher)
- Compact, customizable
- Speed support from 100 Mb/s to more than 10 Gb/s
- Delivered with a full featured reference design

GigE Vision is a standard communication protocol for vision applications based on the well-known Ethernet technology. It allows easy interfacing between GigE Vision devices and PCs running TCP/IP protocol family. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the GigE Vision interface. Due to the speed of GigE Vision, especially at speeds higher than 1 Gb/s, senders and receivers require a fast FPGA-based implementation of the embedded GigE core. GigE Vision cores compatible with Xilinx 7 Series devices (and higher) and Intel Cyclone V devices (and higher).

Working Reference Design

Sensor to Image GigE Vision FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.

Top Level Design

The first component of the IP Core is the **Top Level Design**. It is an interface between external hardware (imager, sensors, GigE PHY) and FPGA internal data processing. We deliver this module as VHDL source code that can be adapted to custom hardware.

Video Acquisition Module

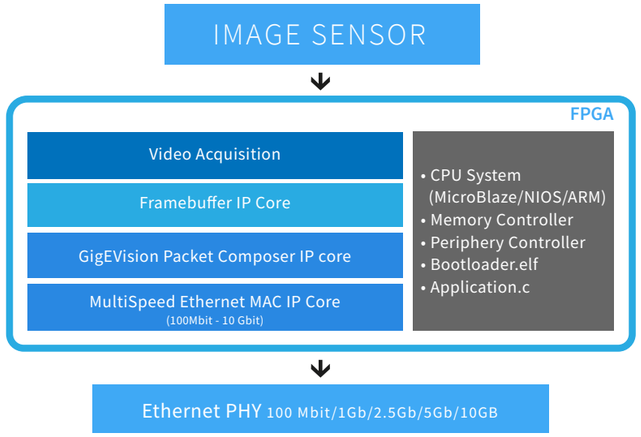
The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which has to be replaced by a sensor interface and pixel processing logic in the camera design.

Framebuffer

The **Framebuffer** core interfaces to the FPGA vendor specific memory controller. The framebuffer allows frame buffering and image partitioning. This is necessary to implement the GigE Vision packet resend function.

GigE Packet Composer

The **GigE Packet Composer** sends all data to the Ethernet MAC and implements the high-speed GigE Vision Streaming Protocol (GVSP).



FPGA Integrated CPU

An **FPGA integrated CPU** (MicroBlaze, NIOS, ARM) handles non-time-critical network and configuration tasks and runs the GigE Vision Control Protocol (GVCP). This software is written in C and can be extended by the customer.

Custom Configuration

Some parts of the design are delivered as compiled files only (for example the GigE Vision control protocol library), while other parts are delivered as source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured either as a GigE Vision camera system with an optional CMOS imager, or as an embedded GigE Vision host (receiver). This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** is a flexible evaluation platform for machine vision applications. It supports GigE Vision host and device reference designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.

NBASE-T interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX-7	ZYNQ-7	ZYNQ ULTRASCALE+	CYCLONE-5
Video Acquisition Interface (Device)	Simple CMOS imager interface or test pattern generator	•	•	•	•
FB-AXI encrypted VHDL (Device)	External memory based streaming buffer, uses Xilinx or Intel-AXI memory controller	•	•	•	•
Framebuffer Linescan support	Support of variable blocksizes often used in linescan applications	o	o	o	o
GigE Vision Packet DeComposer encrypted VHDL (Host)	GigE Vision streaming protocol packet receiver	•	•	•	•
GigE Vision Packet Composer encrypted VHDL (Device)	GigE Vision streaming protocol packet composer	•	•	•	•
TRI Mode MAC encrypted VHDL	10/100/1000 Mbit/s Ethernet MAC	•	•	•	•
10G MAC encrypted VHDL	2,5/5/10Gbit/s Ethernet MAC	o	o	o	o
IEEE1588 Support	Support for the IEEE1588 time synchronisation protocol (master/slave)	o	o	o	o
ACTION Command	Support for low latency GigE Vision Action command encoder and decoder	o	o	o	o
GenDC Frontend (Device)	Support of GigE Vision GenDC Payload Type	o	o	o	o
FPGA CPU Bootloader	GigE Vision bootloader application				
Object file		•			•
C source code		o			o
FPGA CPU GigE Vision application source	GigE Vision user application	•	•	•	•
FPGA CPU GigE Vision library	GigE Vision control protocol library				
Object file		•	•	•	•
C source code		o	o	o	o
FPGA CPU Linux driver	Linux driver for the GigE Vision core	o	o	o	o

RESOURCE USAGE

MODULE	ARTIX-7	ZYNQ-7	ZYNQ ULTRASCALE+	CYCLONE-5
Top Level and Video aquisition interface - Test pattern generator				
Registers	595	555	661	596
Lookup Tables	487	308	441	564
BlockRAMs	0	0	0	0
CPU System -µBlaze/ARM/NIOS/RISC5 based CPU system				
Registers	9177	1392	890	4448
Lookup Tables	10389	1031	596	4068
BlockRAMs	10	0	0	10
DSP	3	0	0	3
FB-AXI - External memory based streaming buffer, uses Xilinx or Intel AXI memory controller				
Registers	5747	5901	5843	4615
Lookup Tables	4203	4333	4203	3167
BlockRAMs	11	15	11	15
DSPs	1	1	1	1
GigE Vision Packet composer - GigE Vision streaming protocol packet composer				
Registers	4808	4681	4701	5221
Lookup Tables	2925	2842	2705	3377
BlockRAMs	9	9	9	9
Tri Mode Ethernet MAC				
Registers	1224	1224	1224	1204
Lookup Tables	868	867	868	729
BlockRAMs	3	5	3	4

GIGE VISION HOST SOFTWARE

SOFTWARE MODULE	WIN7	WIN10	LINUX (UBUNTU LTS)	MAC OS
GigE Vision filter driver				
No sources	•	•	o	o
C-sources	o	o	o	o
GigE Vision library				
Object file	•	•	o	o
C-sources	o	o	o	o
GigE Vision Sphinx Viewer application				
C-sources	•	•	o	o

LEGEND

Included	•
Optional	o
Please contact us	-

USB3 Vision IP Core

USB3 VISION IP CORE FOR FPGA

AT A GLANCE

- Compatible with Xilinx 7 Series (and higher) and Intel Cyclone V devices (and higher)
- Compact, customizable
- Delivered with a working reference design

USB3 Vision is a standard communication protocol for vision applications based on the widely used USB 3.0 interface. As the protocol is standard and supports GenICam, it allows easy interfacing between cameras and PCs. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the USB3 Vision interface. Due to the speed of USB3 Vision, senders and receivers require a fast FPGA-based implementation of the embedded USB core. USB3 Vision cores compatible with Xilinx 7 Series devices (and higher) and Intel Cyclone V devices (and higher).

Working Reference Design

Sensor to Image USB3 Vision FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.

Top Level Design

The first component of the IP Core is the **Top Level Design.** It is an interface between external hardware (imager, sensors, USB3 PHY) and FPGA internal data processing. We deliver this module as VHDL source code and it can be adapted to custom hardware.

Video Acquisition Module

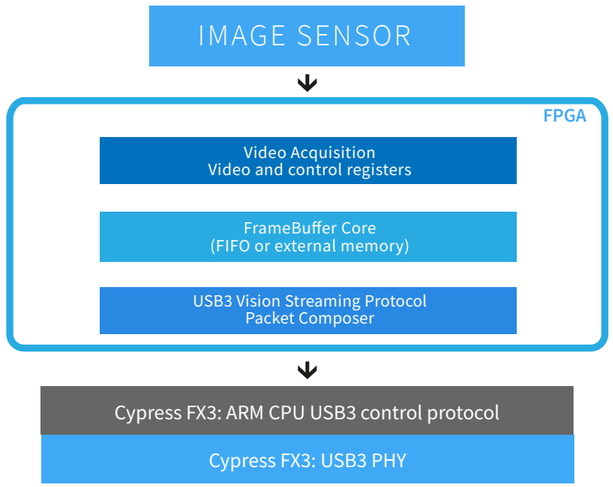
The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which is easily replaced by a sensor interface and pixel processing logic in the camera design.

USB3 Vision Streaming Protocol Packet Composer

The **USB3 Vision Streaming Protocol Packet Composer** takes all data from the video source and builds the USB3 Vision streaming packets. It also handles all low-level communication to the USB3 PHY.

Framebuffer Core

The **Framebuffer core** interfaces to the FPGA vendor specific memory controller. The framebuffer is used for leveling out communication delays between camera and PC.



Cypress FX3

A **Cypress FX3** chip (with integrated ARM CPU and physical interface) is used to handle all USB3 initialization routines and USB3 Vision control channel communication.

Custom Configuration

Some parts of the design are compiled files only (for example the USB3 Vision control protocol library), while other parts are source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured as a USB3 Vision camera system with an optional CMOS imager.

This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** allows is flexible evaluation platform for machine vision applications. It supports USB3 Vision device designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.

USB3 interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX-7	ZYNQ-7	CYCLONE-5
Video aquisition interface	Simple CMOS imager interface or test pattern generator	•	•	•
FB-FIFO	BlockRAM based streaming buffer			
Encrypted VHDL		•	•	•
VHDL source code		o	o	o
FB-AXI encrypted VHDL	External memory based streaming buffer, uses Xilinx or Intel-AXI memory controller	o	o	o
USB3 Vision Packet composer	USB3 Vision streaming protocol packet composer			
Encrypted VHDL		•	•	•
VHDL source code		o	o	o
FX3 USB3 Vision application sources	USB3 Vision user application	•	•	•
FX3 USB3 Vision library	USB3 Vision control protocol library			
Object file		•	•	•
C source code		o	o	o

RESOURCE USAGE

MODULE	ARTIX-7	ZYNQ-7	CYCLONE-5
Top Level and Video aquisition interface - Test pattern generator			
Registers	622	623	679
Lookup Tables	381	424	551
BlockRAMs	0	0	0
CPU System - µBlaze/ARM/NIOS based CPU system with AXI memory controller			
Registers	7642	1897	3523
Lookup Tables	8864	1564	3341
BlockRAMs	6	1	49
DSP	3	0	3
FB-FIFO - BlockRAM based streaming buffer (64kB)			
Registers	1892	1890	2038
Lookup Tables	811	808	1077
BlockRAMs	16	16	64
DSP	5	5	4
FB-AXI - External memory based streaming buffer, uses Xilinx or Intel AXI memory controller			
Registers	4360	4326	4615
Lookup Tables	3296	3284	3167
BlockRAMs	6	6	15
USB3 Vision Packet composer - USB3 Vision streaming protocol packet composer			
Registers	2743	2727	2936
Lookup Tables	2127	2117	2386
BlockRAMs	1	1	4

USB3 VISION HOST SOFTWARE

SOFTWARE MODULE	WIN7	WIN10	LINUX (various distros)	MAC OS
USB3 Vision driver				
No sources	•	•	o	-
C-sources	o	o	o	-
USB3 Vision library				
Object file	•	•	o	-
C-sources	o	o	o	-
USB3 Vision Sphinx Viewer application				
C-sources	•	•	o	-

LEGEND

Included	•
Optional	o
Please contact us	-

CoaXPress IP Core

COAXPRESS IP CORE FOR FPGA

AT A GLANCE

- Compatible with Xilinx 7 Series (and higher), Intel Cyclone V devices (and higher) and Microchip Polarfire Series
- Compact, customizable
- Speed support from 1 Gb/s to more than 50 Gb/s
- Delivered with a working reference design

CoaXPress is a standard communication protocol for vision applications based on widely used coaxial cables. It allows easy interfacing between cameras and frame grabbers and supports the GenICam software standard. Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products using the CoaXPress interface. Due to the speed of CXP, senders and receivers require a fast FPGA-based implementation of the CXP core, preferably using embedded transceivers. CXP cores are compatible with Xilinx 7 series devices (and higher), Intel Cyclone V devices (and higher) and Microchip Polarfire Series.

Working Reference Design

Sensor to Image CXP FPGA solution is delivered as a **working reference design** along with FPGA IP cores. This minimizes development time and allows for top-notch performance at a small footprint, while leaving enough flexibility to customize the design. Sensor to Image cores are compact and leave enough space in the FPGA for your application.

Top Level Design

The first component of the IP Core is the **Top Level Design**. It is an interface between external hardware (imager, sensors, CXP PHY) and FPGA internal data processing. We deliver this module as VHDL source code that can be adapted to custom hardware.

Video Acquisition Module

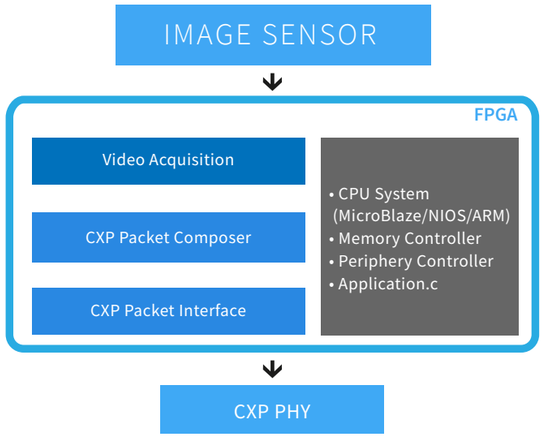
The **Video Acquisition Module** of the reference design simulates a camera with a test pattern generator. This module is delivered as VHDL source code, which has to be replaced by a sensor interface and pixel processing logic in the camera design.

CoaXPress Streaming Interface

The **CXP Streaming Interface** receives all data from the video sensor output to the CXP PHY. It reaches the full speed on the streaming channel according to the CXP specification.

CoaXPress Control Interface

The **CXP Control Interface** receives and sends all data from the CXP control channel, from and to the CXP PHY and implements the control channel according to the CXP specification.



FPGA Integrated CPU

An **FPGA integrated CPU** (MicroBlaze, NIOS, ARM) is used for several non-time-critical control and configuration tasks on the CXP-receiver or transmitter core. This software is written in C and can be extended by the customer.

Custom Configuration

Some parts of the design are compiled files only (for example the CXP control protocol library), while other parts are source code. The design framework comes with all the necessary design files and cores, Vivado or Quartus project files. It is configured either as a CXP camera system with an optional CMOS imager, or as an embedded CXP host (receiver). This system is used as a **reference design** and **evaluation board**. The reference design uses the Xilinx or Intel development tools (not in the scope of delivery).

Sensor to Image **MVDK development kit** is a flexible evaluation platform for machine vision applications. It supports CoaXPress host and device reference designs and various Enclustra™ FPGA modules with Intel and Xilinx FPGAs.

CXP interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ZYNQ7	KINTEX ULTRASCALE	ZYNQ ULTRASCALE+	CYCLONE -10	POLARFIRE
Video Acquisition Interface (Device)	Simple CMOS imager interface or test pattern generator	•	•	•	•	•
CXP Packet DeComposer (Host Core)	CoaXPress streaming protocol packet receiver					
Encrypted VHDL		•	•	•	•	•
VHDL source code		o	o	o	o	o
CXP Packet Composer (Device Core)	CoaXPress streaming protocol packet composer					
Encrypted VHDL		•	•	•	•	•
VHDL source code		o	o	o	o	o
CXP12 Speed Support	Support for CXP12 with 64bit pixel interface	o	o	o	o	o
FPGA CPU CoaXPress application source	CoaXPress user application	•	•	•	•	•
CXP over Fiber Bridge	Converter module to use fiber optics medium with CoaXPress.	o	o	o	o	o
FPGA CPU CoaXPress library	CoaXPress control protocol library					
Object file		•	•	•	•	•
C source code		o	o	o	o	o

RESOURCE USAGE

MODULE	ZYNQ7	KINTEX ULTRASCALE	ZYNQ ULTRASCALE+	CYCLONE-10	POLARFIRE
Top Level and Video aquisition interface Test pattern generator					
Registers	473	445	445	575	476
Lookup Tables	338	290	288	579	743
BlockRAMs	0	0	0	1	0
CPU System -µBlaze/ARM/NIOS/RISC 5 based CPU system					
Registers	987	3051	835	3621	16838
Lookup Tables	708	3236	558	3663	24214
BlockRAMs	0	16	0	42	42
DSP	0	3	0	3	2
CXP Packet composer (Device Core)					
Registers	9794	9701	11640	11152	14881
Lookup Tables	7829	7606	9109	11461	16985
BlockRAMs	15	15	15	60	86
Transceiver	4	4	4	4	4
CXP Packet Decomposer (Host Core)					
Registers	6394	6280	8722	8722	tbd
Lookup Tables	5297	5159	7171	7171	tbd
BlockRAMs	18	18	18	18	tbd
Transceiver	4	4	4	4	tbd

LEGEND

Included	•
Optional	o
Please contact us	-

IMX Pregius IP Core

IP CORE FOR SONY IMX PREGIUS SUB-LVDS IMAGE SENSORS

AT A GLANCE

- Sub-LVDS readout and decoding block
- SPI-based sensor configuration module
- Software library for sensor configuration
- Free running or triggered readout modes

The IMX Pregius from Sony is a series of widely used, high quality CMOS image sensors. ***Sensor to Image*** *IMX Pregius IP Core reads image data efficiently and controls the sensor operations. It is delivered as a reference design along with an FMC module compatible with* ***Sensor to Image*** *MVDK and standard FPGA evaluation kits. Together, they provide an easy way to design a camera.*

SubLVDS Receiver and Deserializer

The **Sub-LVDS Receiver and Deserializer** block is connected to the sensor's output pins and uses the FPGA IO cells to deserialize the image stream. This block is FPGA dependent and currently available for Xilinx FPGAs. The parallel video stream can be cropped and is presented in a Camera Link-like format for further processing.

Trigger Generator

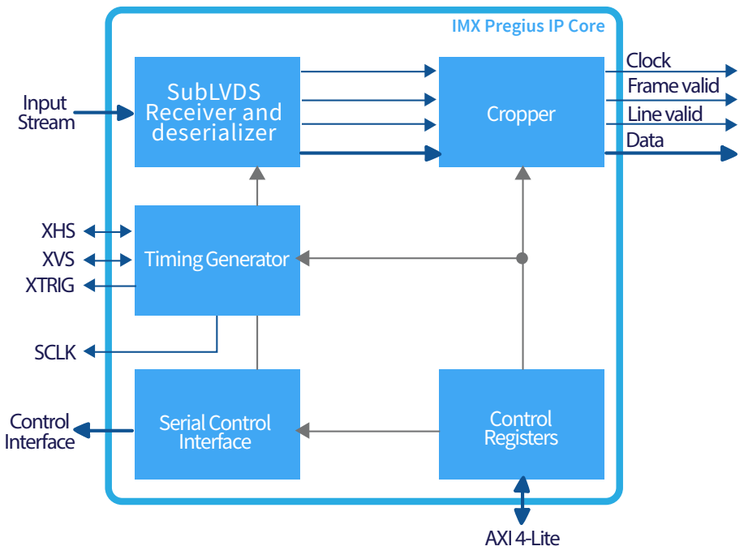
The IMX Pregius sensor itself can be used in free running mode or in slave mode using the core's **timing and trigger generator**. An SPI-based control interface enables sensor configuration, following the correct configuration timing.

Control Registers

The functionality of the IP core is configured either by parameters at compile time, or by **Control Registers** using an AXI-Lite interface at run time. A C software library configures the sensor and the IP core.

Delivery

The IP core is **delivered with a full reference design**, including an FMC (FPGA Mezzanine Card), which forms the interface between the sensor and a standard FPGA evaluation board. The FMC module is FMC-LPC compliant and does all power and level adaptations required by the IMX Pregius CMOS sensor.



MVDK with IMX Pregius interface board

AVAILABLE MODULES

MODULE	DESCRIPTION	ARTIX7 KINTEX7 ZYNQ7	ZYNQ ULTRASCALE+
IMX IP Core	Sub-LVDS IMX Pregius IP		
Encrypted VHDL		•	•
VHDL source code		o	o
IMX IP Software library	API to control core and imager		
Object File		•	•
C source code		o	o
Reference design with GigE Vision interface		•	•

RESOURCE USAGE

MODULE	ARTIX7 KINTEX7 ZYNQ7	ZYNQ ULTRASCALE+
IMX IP Core configured for 4 channels, 12bit pixels		
Registers	1605	1785
Lookup Tables	1756	1978
BlockRAMs	1	1
IMX IP Core configured for 8 channels, 12bit pixels		
Registers	2301	2661
Lookup Tables	2351	2820
BlockRAMs	1	1
IMX IP Core configured for 16 channels, 12bit pixels		
Registers	3534	4254
Lookup Tables	3488	4453
BlockRAMs	1	1

Included	•
Optional	o
Please contact us	-

AVAILABLE SENSOR

MODULE	SENSOR BOARD AVAILABLE	SOFTWARE SUPPORT
IMX174	✓	✓
IMX249	✓	✓
IMX302	✓	✓
IMX252	✓	✓
IMX265	✓	✓
IMX250	✓	✓
IMX264	✓	✓
IMX255	✓	✓
IMX267	✓	✓
IMX305	✓	✓
IMX253	✓	✓
IMX304	✓	✓
IMX273	✓	✓
IMX287	✓	✓

MIPI CSI-2 Receiver IP Core

IP CORE FOR MIPI CSI-2 IMAGERS

AT A GLANCE

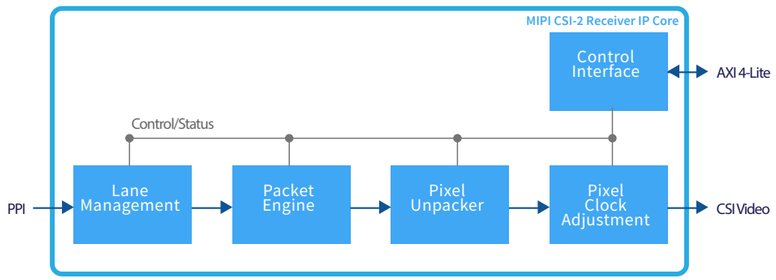
- MIPI CSI-2 receiver and decoding block
- Configurable number of MIPI Lanes
- Using Xilinx D-PHY IP
- Delivered with a reference design for fast development

In the machine vision industry, imagers using the MIPI CSI-2 interface get more and more popular. Many applications require the connection to an FPGA for advanced image pre-processing and further transfer to a host system. Sensor to Image's MIPI CSI-2 Receiver IP core provides a solution for decoding video streams from MIPI sensors in FPGAs. It requires a companion IP core implementing the MIPI D-PHY physical interface. The D-PHY receiver is connected to the CSI-2 receiver using the PHY-Protocol Interface (PPI). In order to shorten the development time, the MIPI CSI-2 Receiver IP core is delivered with a fully working reference design including Sensor to Image's MVDK and an IMX274 MIPI FMC module.

Main features

- FPGA technology independent
- PPI interface to connect to different D-PHY implementations
- Configurable to 1, 2 or 4 data lanes
- Any lane rate supported
- RAW8, RAW10, RAW12, RAW14, RAW16 standard MIPI data types supported
- Embedded data decoding supported
- Direct output of reordered byte stream without pixel unpacking supported
- AXI4-Lite slave control interface

The core is made of five main parts. The lane management together with the packet engine receive parallel byte lanes, extract control information, implement lane alignment and byte reordering, and finally provide aligned payload byte streams. The pixel unpacker extracts pixel data types out of these byte streams. The output pixel clock adjustment converts the pixel stream into the output clock domain. The control interface contains a set of control and status registers accessible by a CPU using the AXI4-Lite slave interface.



Delivery

The core is delivered with a complete reference design for S2I's MVDK with a Zynq Ultrascale+ FPGA, an IMX274 MIPI FMC module and a GigE Vision output. Since the physical interface is abstracted by the Xilinx D-PHY core, it is easy to port the design to other FPGA platforms like for example the 7 series Xilinx FPGAs.

Modules available

The MIPI CSI-2 Receiver IP Core is delivered as encrypted VHDL. It is optionally available as VHDL source code. It is compatible with Xilinx Artix7, Kintex7, Zynq7 and Ultrascale+ FPGAs.

The MIPI CSI-2 Receiver IP Software library is delivered as an object file. It is optionally available as C source code.

MVDK with MIPI CSI-2 Receiver interface board

RESOURCE USAGE

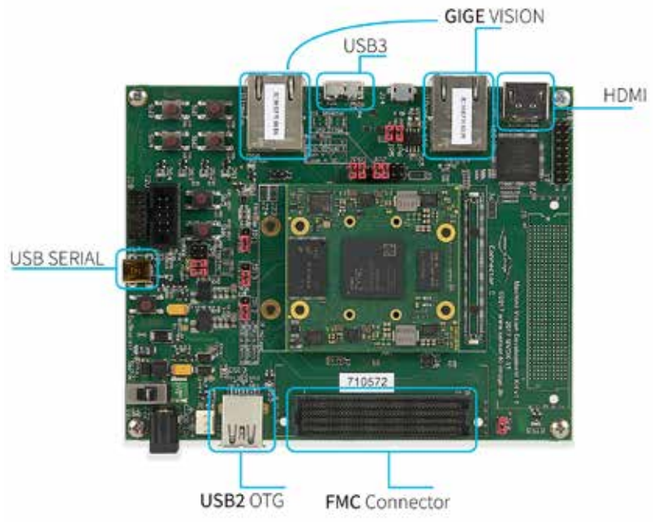
MODULE	ARTIX7 KINTEX7 ZYNQ7	ZYNQ ULTRASCALE+
Xilinx MIPI D-PHY 4 lanes		
External signal level conversion needed (for example Meticom chipset)	Yes	No
Registers	840	1188
Lookup Tables	2157	2261
BlockRAMs	0	0
MIPI CSI-2 Receiver IP Core configured for 4 lanes, 8-bit pixels		
Registers	793	793
Lookup Tables	286	285
BlockRAM	1	1

MVDK

MACHINE VISION DEVELOPMENT KIT

AT A GLANCE

- All major machine vision interfaces available on a single development board
- GigE Vision, CoaXPress and USB3 Vision compliant platform
- Sony IMX Pregius evaluation platform
- GigE Vision up to 10 Gb/s. CoaXPress up to CXP-12
- Support for Enclustra Mercury FPGA modules with Xilinx and Intel FPGAs



Sensor to Image MVDK (Machine Vision Development Kit) is a hardware platform that eases the evaluation and development of products based on S2I's IP Cores and using any major industrial vision interface. The MVDK base board is highly configurable through the use of FMCs (FPGA Mezzanine Cards). It provides an interface to vision sensors and enables the development of GigE Vision, USB3 Vision and CoaXPress cameras (devices), as well as the design of GigE Vision and CoaXPress hosts.

The MVDK is delivered with an Enclustra Mercury FPGA module and an FMC interface board . They come along with a reference design for the selected transport layer interfaces. Together, they minimize development time and allow for top-notch performance at a small footprint, while leaving enough flexibility to customize the design.

For CoaXPress development

The MVDK delivered for CoaXPress development includes an FMC with two or four CXP-6 or CXP-12 links for device (camera) or host (frame grabber) design. The device and host reference designs are fully CoaXPress compliant and certified by the JIIA.

For USB3 Vision development

The MVDK available for USB3 Vision development is based on the 5-Gbit/s technology of standard USB3 components and allows for the most cost-effective high-speed camera design today. The USB3 Vision IP Core development kit is fully compliant with Genicam and certified by the AIA. This is the easiest way to start the design of a new USB3 Vision camera. The USB3 Vision interface is implemented using an FMC designed by Sensor to Image that uses a Cypress FX3 USB3 chip.

For GigE Vision development

The MVDK delivered for GigE Vision development supports the design of camera and host applications compliant with the AIA GigE Vision specification with a speed of up to 10 Gbit/s. 2.5, 5 and 10 Gbit/s applications require a Sensor to Image NBase-T FMC module.

For IMX Pregius development

Sensor to Image MVDK is compliant with Sony's IMX Pregius sensor series, a widely used, high-quality CMOS series of imagers. Sensor to Image supports these sensors with dedicated IP to read data from and control the sensors. The reference design consists of the IMX IP Core together with a GigE Vision compliant output.

For MIPI CSI-2 development

The MVDK delivered with the MIPI CSI-2 receiver IP Core supports the design of cameras with the widely used, high-quality imagers compliant with MIPI CSI-2 standard. Sensor to Image supports reading data from and control the sensors. The reference design consists of the MIPI CSI-2 receiver IP Core together with a GigE Vision compliant output.

MULTIPLE ENCLUSTRA MERCURY MODELS AVAILABLES:

MVDK SA1

MVDK BOARD WITH ENCLUSTRA MERCURY SA1 MODULE
Altera Cyclone V ARM Processor-based SoC FPGA
1 GByte DDR3L SDRAM
64 MB quad SPI Flash
10/100/1000 Ethernet PHY
Five 3.125 Gb/s transceivers

MVDK ZX5

MVDK BOARD WITH ENCLUSTRA MERCURY ZX5 MODULE
Xilinx Zynq-7000-series SoC FPGA 7015
1 GB DDR3 SDRAM
512 MB NAND Flash
64 MB quad SPI Flash
10/100/1000 Ethernet PHY
Four 6.25 Gb/s transceivers

MVDK XU1

MVDK BOARD WITH ENCLUSTRA MERCURY+ XU1 MODULE
Xilinx Zynq Ultrascale+ MPSoC XCZU6
2 GB DDR4 ECC SDRAM
64 MB quad SPI Flash
16 GB eMMC Flash
10/100/1000 Ethernet PHY
8+3 16 Gb/s transceivers (using both FMC connectors)

**note: please ask for other configurations*

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